CLAIMS

1. A method for measuring semiconductor constituent element content comprising the step of obtaining a C content of an SiGeC layer based on a film thickness of the SiGeC layer formed on a semiconductor substrate, the film thickness being obtained by evaluation using spectroscopic ellipsometry, and a measured infrared absorption spectrum of the SiGeC layer.

2. The method for measuring semiconductor constituting element content according to Claim 1, wherein the step of obtaining the C content of the SiGeC layer comprises the steps of:

calculating unit integrated intensity obtained by normalizing integrated intensity at a peak portion of the infrared absorption spectrum by the film thickness of the SiGeC layer; and

extracting the C content corresponding to the calculated unit integrated intensity.

3. The method for measuring semiconductor constituent element content according to Claim 2, wherein the step of extracting the C content corresponding to the unit integrated intensity is carried out based on linear correlation showing the relation between the measured unit

integrated intensity and the C content.

4. The method for measuring semiconductor constituent element content according to Claim 1, wherein obtaining the film thickness of the SiGeC layer comprises the step of using a reference model for an SiGe layer.

5. The method for measuring semiconductor constituent element content according to Claim 1 further comprising the steps of:

obtaining an apparent Ge content of the SiGeC layer by evaluation using spectroscopic ellipsometry; and

obtaining an actual Ge content of the SiGeC layer based on the apparent Ge content and the C content.

6. The method for measuring semiconductor constituent element content according to Claim 5, wherein the step of obtaining the actual Ge content of the SiGeC layer is carried out based on linear correlation showing the relation between the measured apparent Ge content and the C content.

7. The method for measuring semiconductor constituent element content according to Claim 5, wherein the step of obtaining the actual Ge content of the SiGeC layer

comprises the steps of:

obtaining a plurality of correlated straight lines using a parameter of the actual Ge content, which show the relation between the apparent Ge content and the C content;

calculating slope of each correlated straight line;

approximating to a curve the relation between the actual Ge content and the slope of the each correlated straight line; and

calculating the actual Ge content based on the apparent Ge content and the C content using the approximated curve.

8. A method for manufacturing a semiconductor device comprising the steps of:

establishing a chip area and a monitor area on a semiconductor substrate;

forming an SiGeC layer in the chip area and the monitor area;

obtaining a film thickness and an apparent Ge content of the SiGeC layer formed in the monitor area by evaluation using spectroscopic ellipsometry;

obtaining C content of the SiGeC layer based on the film thickness of the SiGeC layer and the measured infrared absorption spectrum of the SiGeC layer;

obtaining an actual Ge content of the SiGeC layer based on the apparent Ge content and the C content; and

feeding back the evaluation data of the obtained C content, actual Ge content and film thickness of the SiGeC layer to growth conditions for the SiGeC layer.

9. The method for manufacturing a semiconductor device according to Claim 8, wherein the step of feeding back the evaluation data to the growth conditions of the SiGeC layer comprises the step of correcting the growth conditions of the SiGeC layer when any predetermined deviation is found by comparing the C content, the actual Ge content, and the film thickness of the SiGeC layer with a preset reference value for each.

10. The method for manufacturing a semiconductor device according to Claim 8, wherein the chip area and the monitor area are individually related to any of a plurality of areas that are formed by being divided after the semiconductor device is manufactured.

11. The method for manufacturing a semiconductor device according to Claim 8, wherein the chip area and the monitor area coexist with any of a plurality of areas that are formed by being divided after the semiconductor device

is manufactured.

12. The method for manufacturing a semiconductor device according to Claim 8, wherein the monitor areas are provided in two or more divided areas.

13. The method for manufacturing a semiconductor device according to Claim 8, wherein the step of forming the SiGeC layer in the chip area and the monitor area comprises the step of growing the SiGeC layer on the semiconductor substrate and then forming an Si/SiGeC layer by growing an Si layer on the SiGeC layer.

14. The method for manufacturing a semiconductor device according to Claim 13, further comprising the step of forming a hetero junction bipolar transistor in the chip area.

15. The method for manufacturing a semiconductor device according to Claim 8, wherein the step of forming the SiGeC layer in the chip area and the monitor area comprises the step of growing the SiGeC layer on the semiconductor substrate and then forming an SiGe/SiGeC layer by growing an SiGe layer on the SiGeC layer.

16. The method for manufacturing a semiconductor device according to Claim 15, further comprising the step of forming a hetero junction bipolar transistor in the chip area.